Post-Doctoral Position in Embedded Vision Systems

The L@bISEN laboratory of ISEN Yncréa Ouest offers a 24 months of a post-doctoral position with computer vision and embedded system background. L@bISEN is being evaluated favorably by HCERES (Haut Conseil de l'évaluation de la recherche et de l'enseignement supérieur).

Context: The position is devoted to scientific research in the area of vision systems to be embedded on autonomous underwater vehicles in order to enhance their efficiency and intelligence. In particular, a special attention will be paid for tracking, learning and detection (TLD) algorithms along with Convolutional Neural Network (CNN) for recognition. These algorithms will be embedded on heterogeneous target composed of Multi-CPU/FPGA (ex. ZYnq-Ultrascale) evaluation board running with partial dynamic reconfiguration of FPGA.

Work description: TLD algorithm will be implemented on System on Programmable Chip (SoPC) evaluation board. The software components of the architecture (data acquisition) will be implemented on the processor part of the SoPC to have more flexibility, while the programmable logic of the device will be used for blocks that require a higher computational complexity. The starting point of the project is to use an image acquisition system running on the SoPC Ultrascale, and to develop a hybrid real-time system to run pre-partionned parts of the TLD algorithm as tasks. The system must be able to select on the fly which part to run on hardware or software resources. The use of dynamic partial reconfiguration of FPGAs is mandatory in order to allow to allow for the implementation of dynamically switchable tasks on hardware.

Key-words: System on Programmable Chip design, Computer Vision, Partial Dynamic Reconfiguration, Unsupervised Learning, embedded systems

Location and supervision: The candidate will be hosted at the L@bISEN Laboratory of ISEN Yncrea Ouest with an engineer contract of 24 months ruled by French laws. The employer will be ISEN Yncréa Ouest. The candidate will be part of Vision-AD team and will be supervised by professors and assistant professors from Brest and Nantes.

Candidate profile: We are looking for highly motivated talent with a Ph.D. degree (or an equivalent title) in a field that is closely related to digital circuit/system design and computer vision. An experience on partial dynamic reconfiguration of FPGA is highly recommended. In addition, we are looking for a candidate with active participation in research projects and motivation for publication in top conferences and scientific journals. French language skills are not required, English is mandatory.

Deadline to apply: As soon as possible. Start date from September 2020. Contract Duration 24 months (**potentially renewable for permanent position** in Brest, Nantes or Caen). Salary: 31k€ gross salary or more based on experience.

Bibliography:

[1] Z. Kalal, K. Mikolajczyk and J. Matas, "Tracking-Learning-Detection," in *IEEE Transactions on Pattern Analysis and Machine Intelligence*, vol. 34, no. 7, pp. 1409-1422, July 2012, doi: 10.1109/TPAMI.2011.239.

[2] A. Podlubne et al., "Low Power Image Processing Applications on FPGAs Using Dynamic Voltage Scaling and Partial Reconfiguration," 2018 Conference on Design and Architectures for Signal and Image Processing (DASIP), Porto, 2018, pp. 64-69, doi: 10.1109/DASIP.2018.8596910.

[3] M. Nguyen, R. Tamburo, S. Narasimhan and J. C. Hoe, "Quantifying the Benefits of Dynamic Partial Reconfiguration for Embedded Vision Applications," 2019 29th International Conference on Field Programmable Logic and Applications (FPL), Barcelona, Spain, 2019, pp. 129-135, doi: 10.1109/FPL.2019.00029.

Contacts and application: Submit (by keeping all documents in one file) a CV, a cover letter, recommendation letters, and any document that may help your application to:

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